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Gate-All-Around (GAA) Nanosheet and Next-Generation Transistors: Device Architecture, Scaling Challenges, and Emerging Applications

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Abstract:
Gate-all-around (GAA) nanosheet transistors have emerged as the state-of-the-art logic device in the announced foundry roadmaps superseding FinFET architectures and forksheet and complementary FET (CFET) structures are being investigated as possible successors for further transistor scaling. The review critically discusses the published literature on GAA device physics, fabrication, electrical characteristics, reliability, and integration challenges with special emphasis on high-performance computing (HPC) applications. A timeline of GAA technology development from 2000 to 2025 provides a chronological overview of the major breakthroughs along with their technological implications. A first order analytical framework is proposed for the evaluation of the effective channel width, the sub-threshold swing, the drain induced barrier lowering (DIBL) and the natural length. The electrostatic control, design flexibility, scalability, fabrication complexity and potential performance advantages of the planar MOSFET, FinFET, nanowire, nanosheet, forksheet and CFET architectures are systematically compared. Results demonstrate that GAA nanosheets provide better gate control and tunable effective channel width, which will enable continued device scaling and performance optimization. However, these advantages come with challenges in nanosheet release, dimensional variability, parasitic resistance and capacitance, thermal management, process integration and long-term reliability. Reported findings are qualified as experimentally measured, numerically simulated, analytically derived or company reported to preserve evidential rigor. The review also highlights a major evidence gap in the absence of independent, like-for-like HPC benchmarks. HPC suitability thus is a reasoned assessment, not an experimentally proven superiority. Finally, a targeted research agenda links outstanding technical challenges with suitable investigation methods and measurable performance targets for future transistor architectures.

Keywords:
Complementary FET (CFET), Drain-Induced Barrier Lowering (DIBL), Electrostatic Control, FinFET, Forksheet, Gate-All-Around (GAA) Nanosheet Transistors, High-Performance Computing (HPC), Subthreshold Swing, Thermal Management, Transistor Scaling

1. INTRODUCTION

Demand for computing throughput per watt keeps climbing, whether the workload is AI training and inference, scientific computing in an HPC centre, or a phone in someone's pocket. Meeting it takes more transistors, higher drive current, and lower switching energy at the same time. Planar bulk MOSFETs ran into trouble first. With the gate acting on only one face of the channel, a short device lets the drain field reach the source barrier, and drain-induced barrier lowering (DIBL) and subthreshold leakage follow. The FinFET responded by wrapping the gate over a thin fin on three sides [1].

The FinFET has a ceiling of its own. Because width comes in whole fins, designers cannot tune drive strength continuously. Fins must also stay tall and thin as pitches shrink, and fin spacing and parasitic capacitance eat into the standard-cell footprint. Simulations that set FinFETs against gate-all-around nanowires examine exactly these trade-offs in performance, scaling, and variability [2]. Above the device, interconnect resistance and power delivery tighten the squeeze further.

A GAA nanosheet transistor stacks several thin wide silicon sheets and wraps the gate dielectric and metal around each of them [3]. A stack of sheets offers a more effective width for a given footprint than a single fin and since the sheet width is determined by lithography, it can take any value instead of a multiple of the fin pitch [3], [4]. The device is out of the lab, too. In June 2022, Samsung announced the production of 3 nm with its multi-bridge-channel FET (MBCFET) [5]. TSMC says its first nanosheet node, N2, entered volume production in Q4 2025 [6], while Intel describes 18A, which merges RibbonFET with backside power, as in high-volume production [7]. All three are manufacturer statements and have not been audited by an independent and node names, are marketing labels, not dimensions.

Several problems are still open: sheet release, inner-spacer control, leakage under the bottom sheet, parasitic resistance and capacitance, self-heating, and reliability [8], [9]. We report no new measurements or device simulations. The only computed curves are the analytical estimates in Fig. 4, which come straight from Eq. (4). What the paper offers instead is a timeline of GAA nanosheet innovation with a reasoned view of its fit to HPC, a comparison of architectures and their electrostatics, a synthesis of fabrication, materials, performance, and reliability trade-offs with an evidence-labeled look at emerging devices, and a ranked research agenda. Section 2 follows the architectural lineage and Section 3 the timeline. Sections 4 to 6 cover the nanosheet device, its fabrication, and its performance, Section 7 compares architectures, Section 8 deals with materials and reliability, and Section 9 looks at next-generation devices and applications. Sections 10 and 11 close with research directions and conclusions.

2. EVOLUTION OF CMOS TRANSISTOR ARCHITECTURES

Fig. 1 lines up the gate-channel geometries. A planar MOSFET gates one face. The FinFET adds the two sidewalls of a thin fin, and its first demonstration pushed scaling toward a 20 nm gate length [1]. GAA nanowires go all the way round the channel. Stacked horizontal silicon nanowires with a replacement metal gate on bulk silicon have been built [10], and a simulation study sets such wires against FinFETs [2]. A single nanowire carries current around a small perimeter, which is why widening it into a sheet gives more effective width per footprint [3].

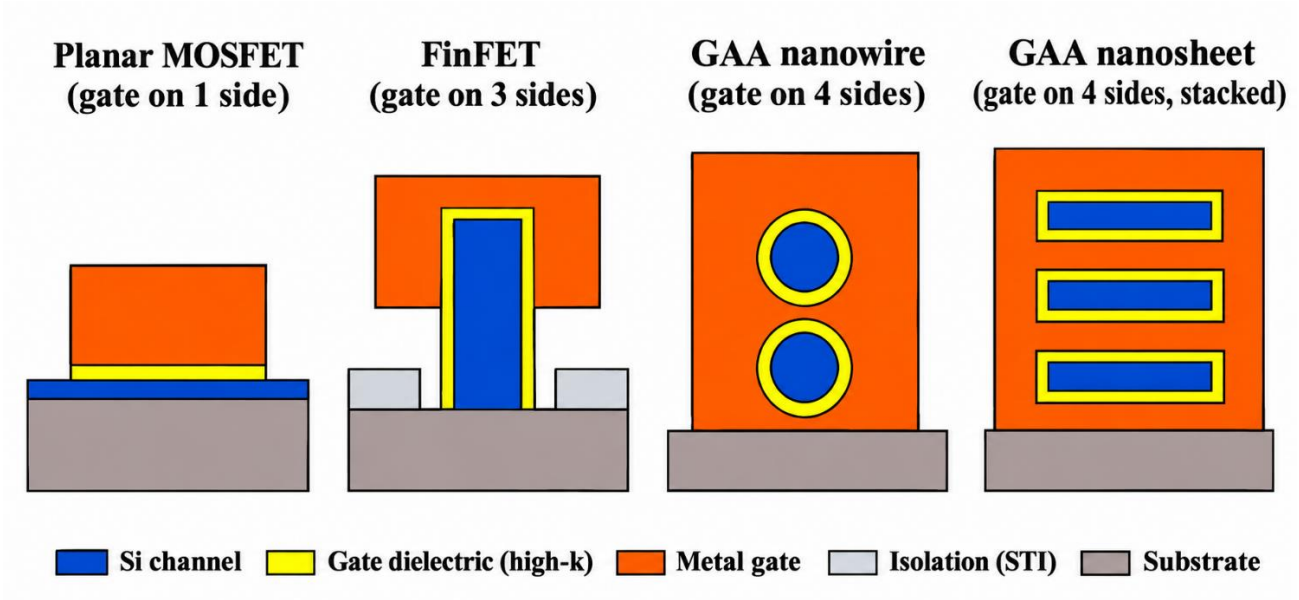


Fig. 1. Evolution of transistor architectures, shown as cross-sections perpendicular to the channel. The gate surrounds one, three, and four sides of the channel in the planar, FinFET, and GAA devices, respectively (Schematic, not to scale).

Two further concepts go beyond the nanosheet. The forksheet places a dielectric wall between n-type and p-type devices so that they can be packed closer [11], and the CFET stacks one polarity on top of the other [12], [13]. Table I compares mainstream and near mainstream options and their status. Only

planar and FinFET devices are mature technologies. The companies cited report volume production of nanosheets. The sources treat nanowires as research demonstrations.

Table 1: Structural and Technological Comparison of Planar, FinFET, Gaa Nanowire, and Gaa Nanosheet Architectures

Architecture	Gate–channel contact	Advantages	Limitations	Status
Planar MOSFET	Top surface only (1 side)	Simplest layout; width set continuously by layout; mature process	Weakest electrostatic control as gate length shrinks, which motivated 3D devices [1]	Established manufacturing technology
FinFET	Fin sidewalls and top (3 sides) [1]	Better gate control than planar; scalable toward 20 nm gate length in the original demonstration [1]	Width quantized by fin count; less width per footprint than stacked sheets [3]	Established manufacturing technology
GAA nanowire	All sides of each wire	Strong electrostatics; stacked-wire flow on bulk Si demonstrated [10]	Small conducting perimeter per wire; compared with FinFET by simulation in [2]	Research demonstrations in the cited work; no volume product cited
GAA nanosheet	All faces of each stacked sheet [3]	More effective width per footprint; width tunable by patterning [3], [4]	SiGe release, inner spacers, bottom-sheet leakage, self-heating, reliability [8], [14]	Company-reported volume production [5], [6], [7]

3. TIMELINE OF GAA NANOSHEET INNOVATION AND SUITABILITY FOR HPC

Fig. 2 and Table II align the milestones on a single time axis. The record is divided into three parts: early concepts (2000-2016), platform building (2017-2020), and production with HPC-oriented tuning (2021-2025). Each entry has an evidence class. Research paper is a report of the devices that have been measured or fabricated . Company reported item is a statement by the manufacturer itself . Sources that explicitly address HPC are flagged with red rings in Fig. 2. This selection includes only those sources we have been able to verify, so it is a representative record, not a complete history.

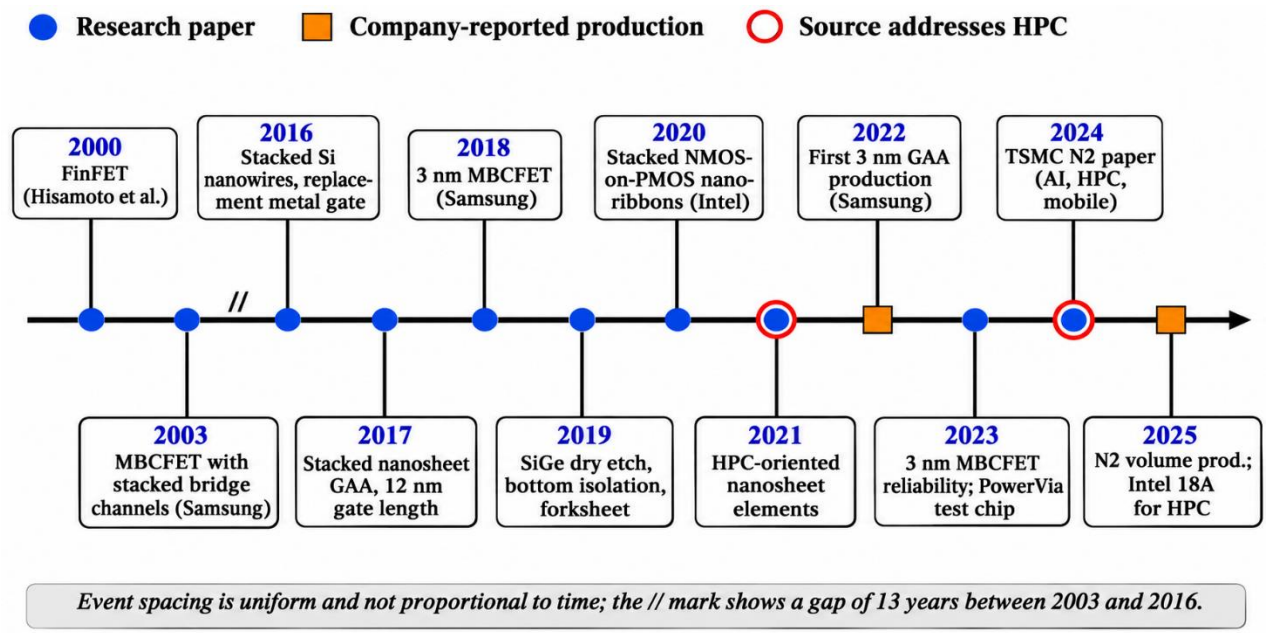


Fig. 2. 2000-2025 Timeline of GAA nanosheet innovation. Blue circles represent research papers, orange squares represent company-reported production milestones, and red rings represent sources that mention HPC explicitly. Events are evenly spaced and the axis is not time proportional. Original figure compiled from the cited sources [1], [15], [10], [3], [4], [11], [13], [16], [5], [17], [18], [19], [6], [20], [7].

3.1 Concepts and early demonstrations, 2000 to 2016

The 2000 FinFET introduced gate wrap around a thin body [1]. A multibridge-channel MOSFET (MBCFET) with stacked bridge-shaped channels was reported by a Samsung-led group three years later, describing its fabrication and behavior [15]. The sources cited here have nothing from 2003-2016. The gap probably tells us more about our selection than about the field and the record can't settle the point. In 2016, stacked horizontal silicon nanowires with replacement metal gate on bulk silicon have been fabricated [10]. Another work compared the self-heating in FinFET and GAA nanowire devices with Si, Ge, and III/V channels [9]. This was an early clue that heat would limit surrounded channels.

3.2 Platform building, 2017 to 2020

The 2017 stacked nanosheet transistor demonstrated good electrostatics at 12 nm gate length and 44/48 nm contacted poly pitch [3]. A subthreshold swing of 65 mV/decade was reported in the 3nm MBCFET paper of 2018 [4]. In 2019 three enabling pieces arrived: a dry selective SiGe etch for sheet release [21], full bottom dielectric isolation against sub-sheet leakage [22], and the forksheet as an architectural variant [11]. Stacked NMOS-on-PMOS nanoribbons followed in 2020 and brought the CFET idea into hardware [13]. By then the nanosheet was no longer a single demonstration but a set of process modules that a production flow could adopt.

3.3 Production and HPC-oriented tuning, 2021 to 2025

A 2021 paper set out the critical nanosheet elements for HPC technology [16]. In 2022 Samsung announced the first 3 nm GAA production and quoted up to 45% lower power, 23% higher performance, and 16% smaller area against its own 5 nm process [5]. A reliability assessment of the 3 nm MBCFET appeared in 2023 [17], alongside Intel's report of backside power delivery on a product-like test chip in a FinFET process [18]. TSMC published a 2 nm platform in 2024, co-optimized with 3D integration for AI, HPC, and mobile products [19]. In 2025 TSMC stated that N2 had entered volume production in the fourth quarter [6], and Intel presented 18A with RibbonFET and PowerVia for advanced HPC [20]. Intel's web page calls 18A high-volume production and names the Clearwater Forest server processor as a demonstration [7].

Table 2: Milestones In Gaa Nanosheet Development, Evidence Class, And Relevance To HPC

Year	Milestone and source	Evidence class	HPC relevance (assessment unless a source says otherwise)
2000	FinFET, a self-aligned double-gate MOSFET scalable to 20 nm [1]	Research paper (measured devices)	Established the gate-wrap principle that GAA extends; no HPC claim in the source
2003	MBCFET with stacked bridge channels; fabrication and characteristics [15]	Research paper	Assessment: stacked channels are the route to more drive per footprint; no HPC claim in the source
2016	Stacked Si nanowires with replacement metal gate on bulk Si [10]; self-heating of FinFET and GAA nanowires [9]	Research papers	Assessment: bulk-Si flow aids manufacturability; self-heating is relevant to sustained high power density
2017	Stacked nanosheet GAA at 12 nm gate length, 44/48 nm CPP, multiple threshold voltages [3]	Research paper (measured)	Assessment: wide sheets raise drive per footprint (Eq. (1)); multi-V_T options suit mixed speed and power blocks
2018	3 nm MBCFET with 65 mV/decade swing [4]	Research paper; company-reported figures	Source targets low-power and high-performance use; HPC is not singled out
2019	Dry SiGe etch [21]; bottom dielectric isolation [22]; forksheet [11]	Research papers (forksheet by simulation)	Assessment: lower sub-sheet leakage helps power at high drive; forksheet targets cell-area reduction
2020	Stacked NMOS-on-PMOS nanoribbons [13]	Research paper	Assessment: density option beyond nanosheets; thermal and contact issues not quantified in the source
2021	Critical elements of nanosheet technology for HPC [16]	Research paper	Source addresses HPC directly

Year	Milestone and source	Evidence class	HPC relevance (assessment unless a source says otherwise)
2022	First 3 nm GAA production: up to 45% less power, 23% more performance, 16% less area versus the company's 5 nm [5]	Company-reported	Source markets the process for high-performance use; baseline is the company's own 5 nm node, so no architecture-only inference
2023	Reliability assessment of 3 nm MBCFET [17]; PowerVia test chip with over 30% voltage-droop improvement and 6% frequency gain on a FinFET process [18]	Research papers (measured)	Reliability and power delivery matter for HPC; the backside-power gain was shown on FinFETs, not nanosheets
2024	TSMC 2 nm platform with nanosheets and 3DIC co-optimization for AI, HPC, and mobile [19]	Research paper by the manufacturer	Source addresses HPC directly
2025	N2 in volume production since 4Q25 [6]; Intel 18A with RibbonFET and PowerVia for HPC [20], described as in high-volume production, with a 30% density gain over Intel 3.1 [7]	Company-reported	Sources address HPC directly; no independent benchmark among the cited sources

3.4 Suitability for HPC

HPC processors reward high drive current per unit area, tolerance of sustained power density, stable supply voltage, and long life at high temperature. Against those criteria the timeline supports a qualified view. Stacked sheets raise effective width per footprint (Eq. (1)), and continuous width tuning lets designers trade speed against power block by block [3], [4]. Work-function patterning results in multiple threshold voltages [3], and there is an HPC-oriented analysis of nanosheet elements [16]. 3D integration or backside power with nanosheets is used in platforms targeting HPC by TSMC and Intel [19], [20], but the power-delivery benefit measured by Intel was from a FinFET base [18]. Against that, self heating and reliability remain unresolved for continuous high power operation [9], [23], [8], [17].

Suitability is an assessment, not a measurement; There is no cited source that benchmarks nanosheets versus FinFETs for HPC at matched design rules, bias, and workload and company claims are based on different baselines and cannot be ranked against each other. Section 10 lists the measurements that would turn the assessment into evidence.

4. GAA NANOSHEET TRANSISTOR ARCHITECTURE AND OPERATING PRINCIPLES

4.1 Physical structure

Schematic of a stacked GAA nanosheet transistor is shown in figure 3 shown below.

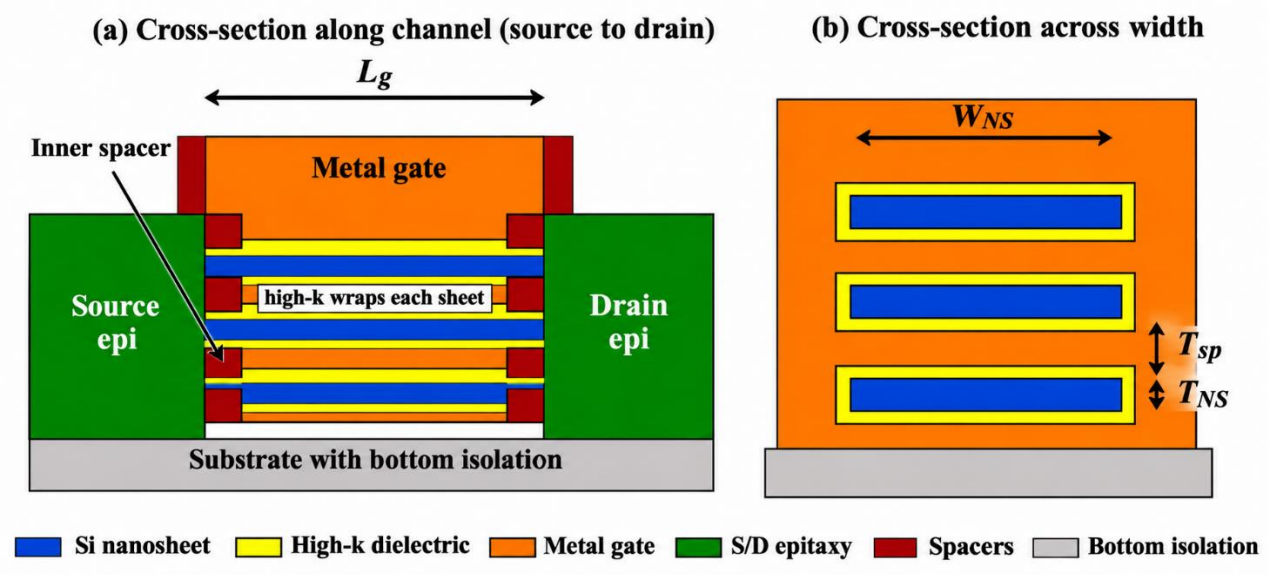


Fig. 3. Schematic of a stacked GAA nanosheet transistor: (a) cross-section along the channel showing the gate stack, three Si nanosheets, source/drain epitaxy, and inner spacers; (b) cross-section across the width showing sheet width W_{NS}, thickness T_{NS}, and spacing T_{sp}. Original schematic, not to scale; the number of sheets is illustrative.

Fig. 3 labels the main elements. Silicon sheets are grown as a superlattice with sacrificial silicon-germanium (SiGe) layers, etched into a multilayer stack, and released so that each sheet hangs between the source and drain epitaxy [3], [14]. The gate stack, an interfacial layer, a high-k dielectric, and work-function metals, fills the space around every sheet. Inner spacers keep the gate away from the source/drain epitaxy at the ends of the gaps [8]. The spacing between sheets, T_{sp}, has to be wide enough to hold the whole gate stack. Published work shows work-function-metal replacement and multiple threshold voltages at aggressive sheet spacing for wide stacked sheets [3], and dielectric isolation beneath the stack suppresses parasitic conduction under the bottom sheet [3], [22].
The effective conducting perimeter sets the drive width. For N_{sheet} identical rectangular sheets,

$$W_{eff} = N_{sheet} \cdot 2(W_{NS} + T_{NS}) \quad (1)$$

where W_{eff} is the effective electrical width, W_{NS} and T_{NS} are the sheet width and thickness, and N_{sheet} is the number of sheets. Eq. (1) assumes a rectangular cross-section, conduction on all four faces with equal mobility, and no corner rounding. Real sheets have rounded corners and face-dependent mobility, so Eq. (1) gives an upper-bound estimate for geometry comparisons and not a calibrated width.

4.2 Electrostatics and figures of merit

A schematic comparison FinFET and GAA nanosheet schematic comparison is given in Fig. 4 below.

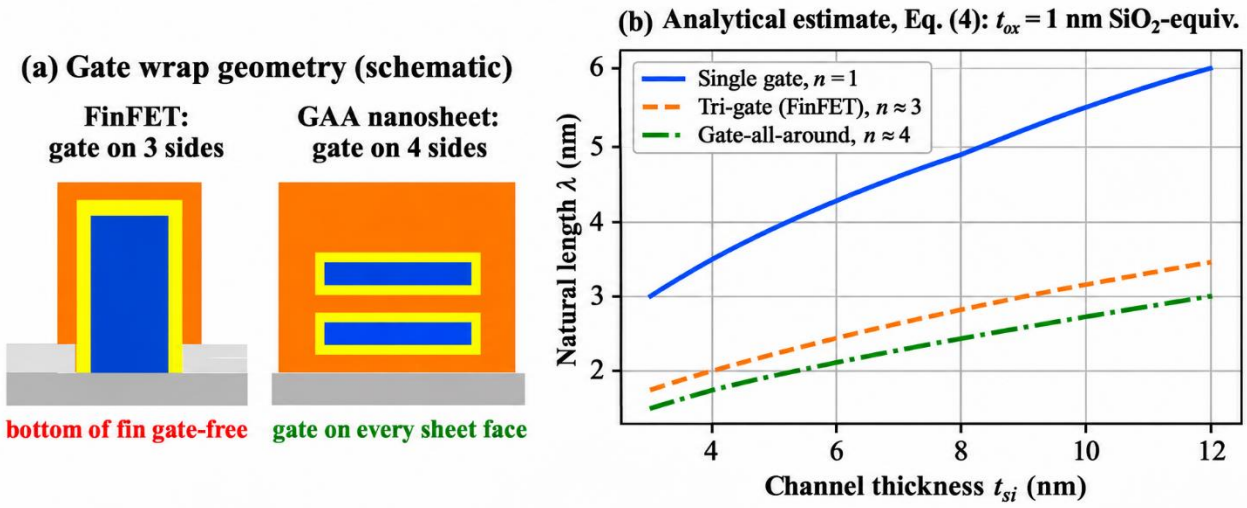


Fig. 4. Gate coverage and electrostatic control: (a) schematic comparison of gate wrap in a FinFET and a GAA nanosheet; (b) natural length from Eq. (4) versus body thickness for single-gate, tri-gate, and GAA effective gate counts. Panel (b) is an analytical estimate computed for this paper under the stated assumptions ($\varepsilon_{Si}/\varepsilon_{ox}$ = 11.7/3.9, t_{ox} = 1 nm), not measured data; the values $n \approx 3$ and $n \approx 4$ are heuristic.

The subthreshold swing of a fully depleted, thin-body device is

$$SS = \frac{kT}{q} \ln 10 \left(1 + \frac{C_d}{C_{ox}}\right) \quad (2)$$

where k is Boltzmann's constant, T the absolute temperature, q the elementary charge, C_d the depletion (body) capacitance, and C_{ox} the gate-dielectric capacitance. At 300 K the ideal limit is about 60 mV/decade, and a device approaches it when C_d/C_{ox} is small, which better gate coverage and a thin body promote. A swing of 65 mV/decade was reported for the 3 nm MBCFET [4]. DIBL is defined as

$$DIBL = \frac{V_{T,lin} - V_{T,sat}}{V_{DS,sat} - V_{DS,lin}} \quad (3)$$

where $V_{T,lin}$ and $V_{T,sat}$ are threshold voltages extracted at the low drain bias $V_{DS,lin}$ and the high drain bias $V_{DS,sat}$. DIBL is quoted in mV/V and only compares between devices when extraction method and biases match.

The natural length describes how quickly the drain potential decays into the channel. Scaling theory for surrounding-gate devices appears in [24]. A commonly used first-order form is

$$\lambda = \sqrt{\frac{\varepsilon_{Si} t_{Si} t_{ox}}{n \varepsilon_{ox}}} \quad (4)$$

where λ is the natural length, ε_{Si} and ε_{ox} are the permittivities of silicon and the gate oxide, t_{Si} is the body thickness, t_{ox} the oxide thickness, and n an effective gate count. We take $n = 1$ for a single gate and $n = 2$ for a double gate, with $n \approx 3$ for a tri-gate and $n \approx 4$ for a GAA structure as heuristic approximations. Eq. (4) assumes a fully depleted, undoped, uniform body and neglects corner effects, quantum confinement, and source/drain geometry. Treat it as a design aid, not a substitute for three-dimensional TCAD or measurement. A smaller λ allows a shorter gate length at the same electrostatic integrity, and as a rule of thumb the gate length should be several times λ. Fig. 4(b) evaluates Eq. (4) for t_{ox} = 1 nm of silicon-dioxide-equivalent thickness. The curves show why extra gate coverage permits either a thicker body or a shorter channel at equal electrostatic control. In measurement, good electrostatics have been reported for stacked nanosheets at a gate length of 12 nm and a contacted poly pitch (CPP) of 44/48 nm [3].

In strong inversion, carrier velocity and not mobility limits the on-current of a short-channel device. A simple estimate is

$$I_{on} \approx W_{eff} C_{ox} v_{sat} (V_{GS} - V_T) \quad (5)$$

where I_{on} is the on-current, C_{ox} the gate capacitance per unit area, v_{sat} the saturation velocity, V_{GS} the gate-source voltage, and V_T the threshold voltage. Eq. (5) assumes velocity saturation along the entire channel and ignores series resistance, so it overestimates measured current. Its value lies in showing that I_{on} scales with W_{eff} from Eq. (1). Transconductance is

$$g_m = \frac{\partial I_D}{\partial V_{GS}} |_{V_{DS}} \quad (6)$$

where g_m is the transconductance and I_D the drain current, evaluated at constant drain bias V_{DS}. The work-function metal, the gate dielectric, and the sheet thickness (through quantum confinement, Section 8) set V_T, and patterning work-function metals between sheets yields multiple V_T options [3].

5. DEVICE FABRICATION AND PROCESS INTEGRATION

Public sources describe the following sequence for horizontal nanosheet devices. Foundry-specific recipes are proprietary and are not assumed here.

1) **Epitaxial growth.** Alternating Si and SiGe layers are grown on the substrate, and layer thickness sets T_{NS} and T_{sp} [3], [14].
2) **Patterning.** Lithography and etch define the multilayer stack. The pattern sets sheet width, which allows continuous width tuning [3], [4].
3) **Sacrificial-layer removal and sheet release.** A replacement-gate flow removes the SiGe selectively and leaves suspended Si sheets. A dry selective SiGe etch has been reported for this step [21].
4) **Inner-spacer formation.** Dielectric spacers form in the recesses between sheets and separate the gate from the source/drain epitaxy [8].
5) **Source/drain epitaxy and integration.** Source/drain regions are grown epitaxially from the sheet ends, and wrap-around contacts have been studied to lower the extrinsic resistance [3].

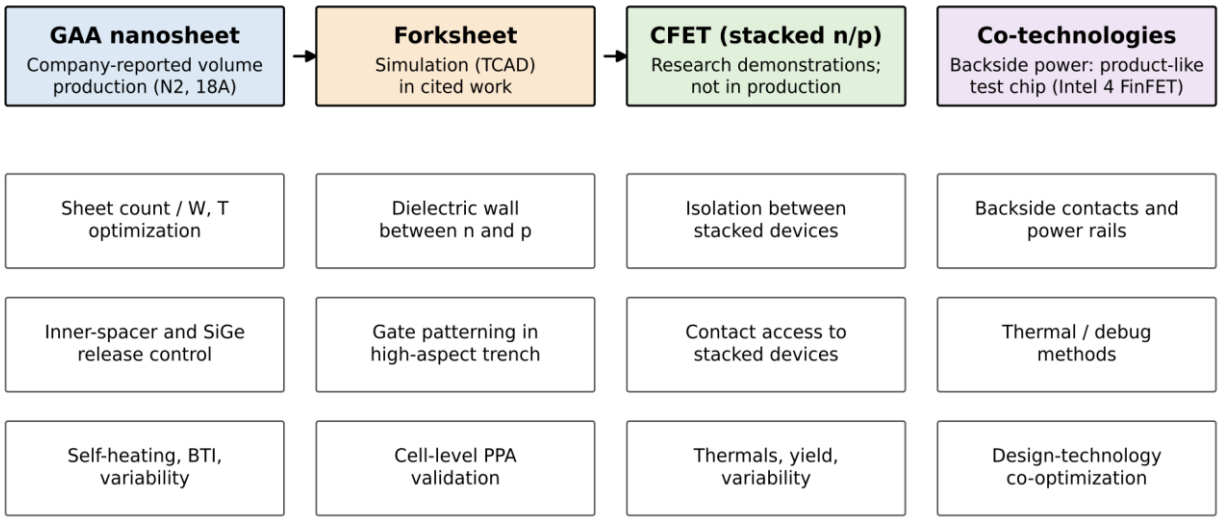
6) **Gate dielectric and metal gate.** A high-k dielectric and work-function metals are deposited around each sheet, and the gate must fill the narrow gaps between sheets [3].
7) **Thermal processing, contacts, and interconnect.** Contact formation and back-end integration follow, and their thermal budget and parasitics affect device performance and reliability [14].

The sequence contains some integration problems. The sheet thickness depends on the epitaxial uniformity and on the selectivity of the SiGe removal. Suspended sheets must stay mechanically stable, and one integration reports eliminating stiction in long-channel devices [3]. The gate stack must fill narrow gaps without damaging interfaces. The bottom sheet must be isolated from the substrate to block a leakage path [22]. Stacking of channels also introduces variability sheet-to-sheet that single-channel devices do not have [2].

Cost and ramp speed matter as much as physics. Samsung stated that its MBCFET reuses roughly 90% of its FinFET fabrication technology and needs only a few revised photomasks [4], which favors a fast ramp and quick yield learning. Added modules such as inner spacers and bottom isolation push the other way [8], [22]. Public sources give no comparable cost or yield figures, so we make no quantitative cost comparison.

6. ELECTRICAL PERFORMANCE AND SCALING CHARACTERISTICS

Any performance number has to be read with its evidence class in mind. The sources contain four: measured device data, calibrated or uncalibrated simulation, analytical estimates, and company-reported or projected figures. Results from different classes, or from different bias, temperature, and extraction conditions, cannot be compared directly.



Conceptual roadmap: arrows show architectural lineage, not performance ranking or schedule. Status text paraphrases cited sources.

Fig. 5. Conceptual roadmap of the architectures and enabling technologies discussed in this paper, with the principal open integration problems under each. Status labels paraphrase the cited sources [6], [7], [11], [13], [18]; arrows show architectural lineage, not performance ranking or schedule.

Switching metrics. Dynamic switching energy and delay follow from the load capacitance C_L, which includes gate and parasitic components, and the supply voltage V_{DD}:

$$E_{sw} = C_L {V_{DD}}^2 \tag{7}$$

$$\tau \approx \frac{C_L V_{DD}}{I_{on}} \tag{8}$$

where E_{sw} is the energy per switching event and τ is a first-order delay. Eqs. (7) and (8) assume a single lumped capacitance and a constant on-current during switching, so they indicate trends and do not predict circuit delay. They show why the higher I_{on} from larger W_{eff} must be weighed against the extra gate and parasitic capacitance of wider and more numerous sheets.

Geometry dependence. Raising N_{sheet} or W_{NS} increases W_{eff} in Eq. (1) and with it I_{on}, but capacitance climbs too, and a wide sheet controls its sidewalls less well than a narrow one. Thinning T_{NS} helps electrostatics (Eq. (4)) at the price of stronger quantum confinement and roughness sensitivity (Section 8). A larger T_{sp} makes gate-stack fill and multi-V_T patterning easier [3], but it reduces the number of sheets that fit in a given stack height and raises parasitic coupling to the source/drain. Shorter L_g tightens every one of these constraints.

Reported results. The figure 5 shown above illustrate the evidence classes and should not be ranked against one another. Measured: stacked nanosheets with good electrostatics at L_g = 12 nm and CPP of 44/48 nm [3]. Company-reported: an MBCFET swing of 65 mV/decade and an on-current gain of 31% over the same company's FinFET [4]; for Samsung's 3 nm process, up to 45% lower power, 23% higher performance, and 16% smaller area against its 5 nm process [5]; and, for Intel 18A, a 30% density improvement over Intel 3.1 [7]. TSMC describes full-node gains in performance and power for N2 without numbers on its web page [6]. Every one of these claims uses a different baseline and covers a whole process node, so none can be credited to the transistor architecture alone. Simulated: forksheet standard-cell results appear in Section 7 [11]. Variability and reliability results appear in [2], [8].

Fig. 5 is a conceptual roadmap rather than a metric plot, because the cited sources share no common definitions, biases, and gate lengths.

7. COMPARATIVE ASSESSMENT OF FINFET, GAA NANOSHEET, AND EMERGING TRANSISTORS

Table III compares the nanosheet with the forksheet, CFET, and vertical-channel concepts. Metrics that the cited sources do not give in comparable form are marked "n/a" and are not estimated.

Table 3: Comparison of GAA Nanosheet, Forksheet, CFET, and Vertical-Channel Architectures

Architecture	Defining feature	Evidence stage	Reported results (class)	Open issues
GAA nanosheet	Stacked horizontal sheets; gate on all faces; n and p side by side [3]	Company-reported volume production [5], [6], [7]	Swing and on-current gain reported for MBCFET (company-reported) [4]; good electrostatics at 12 nm gate length (measured) [3]	Release, inner spacer, bottom isolation, self-heating, reliability [8], [22]
Forksheet	Dielectric wall between n and p nanosheets, allowing tighter n-to-p spacing [11]	Simulation in the cited work [11]	About 10% performance gain and above 20% cell-area reduction versus nanosheet at assumed 2 nm-node rules (simulated, institute-reported) [11]	Experimental validation and standard-cell results: n/a in cited sources
CFET	n-type transistor stacked over p-type (or reverse) on a common gate [12]	Research demonstrations [13]	Stacked nanoribbon NMOS-on-PMOS devices demonstrated [13]; no comparable metrics in the cited sources	Assessment: isolation between stacked devices, contact access, and thermal behavior; not quantified in the cited sources
Vertical-channel FET	Current flows perpendicular to the wafer	Not assessed	n/a: no source cited in this paper	n/a

The nanosheet and the CFET are different kinds of thing. The channel geometry, or how the gate wraps around the semiconductor, is set by the nanosheet. The CFET describes the structure of complementary transistors, and it can have nanosheet or nanoribbon channels [13]. The forksheet is a nanosheet variant with a dielectric wall which changes the n-to-p spacing [11]. Forksheets and CFETs are thus extensions of GAA concepts rather than a replacement. None of the cited sources show either to be better than the nanosheet, with comparisons stopping at simulation or early demonstration.

8. MATERIALS, RELIABILITY, AND MANUFACTURING CHALLENGES

Materials. The selective etch of SiGe defines the sheet thickness [21], [14]. Silicon forms the channel and SiGe the sacrificial layer. The gate stack consists of high-k dielectrics and work-function metals, and the source/drain epitaxy and contact scheme determine the extrinsic resistance [3]. The reliability implications of each element are discussed in a review [8].

Quantum confinement and surface effects. A thin sheet confines carriers along its thickness. In an infinite-well approximation the lowest subband energy rises as

$$\Delta E_1 = \frac{\hbar^2 \pi^2}{2m^* {T_{NS}}^2} \tag{9}$$

where ΔE_1 is the ground-state energy above the band edge, ħ the reduced Planck constant, m^* the confinement effective mass, and T_{NS} the sheet thickness. Eq. (9) assumes an infinite barrier and parabolic bands, so it overstates confinement in real high-k stacks, yet it captures the $1/T_{NS}^2$ trend. When thickness varies, thinner sheets shift the threshold voltage and spoil V_T uniformity. Surface roughness and interface traps lower mobility further, and the different crystal faces on the top and sidewalls of a sheet affect mobility and bias-temperature behavior [8].

Reliability. Reviews of nanosheet reliability name bias-temperature instability (BTI), hot-carrier injection (HCI), gate-oxide time-dependent dielectric breakdown (TDDB), and middle-of-line TDDB as the main mechanisms, with the inner-spacer region as a new feature of the structure [8]. Reliability evaluation of a 3nm MBCFET technology is reported [17]. The self-heating is due to the surrounding dielectrics trapping heat near the channel. One study compares the self-heating of FinFET and nanowire GAA devices with different channel materials [9], and the other one considers the localized thermal effects in GAA devices [23]. Temperature couples self-heating to BTI and HCI, hence the two analyzes cannot be performed separately [8].

Table 4: Major Scaling Challenges, Causes, Mitigation Approaches in the Literature, and Metric

Challenge	Physical cause	Mitigation reported in the literature	Relevant metrics
Sheet release and thickness control	Selective SiGe removal must stop at Si; etch non-uniformity changes T_{NS}	Dry selective SiGe etch [21]; process reviews [14]	Sheet-thickness spread; V_T spread
Bottom-sheet leakage	Parasitic conduction path beneath the lowest sheet	Dielectric isolation on bulk substrates [3]; full bottom dielectric isolation [22]	I_{off}; sub-sheet leakage
Parasitic resistance and capacitance	Small contact area at sheet ends; inner-spacer and gate-to-source/drain geometry	Wrap-around contacts evaluated [3]; spacer engineering [8]	Extrinsic resistance; gate capacitance; delay
Self-heating	Heat confined by surrounding dielectrics and thin sheets	Thermal characterization and thermally aware analysis [9], [23]	Lattice temperature rise; degradation acceleration
BTI, HCI, TDDB	Surface orientation, corner fields, inner-spacer region, high-k stack	Geometry and gate-stack optimization informed by reliability studies [8], [17]	ΔV_T under stress; lifetime
Variability	Sheet-geometry spread and differences among stacked channels	Statistical simulation, shown for nanowire devices [2]	$\sigma(V_T)$; $\sigma(I_{on})$
Confinement and roughness	Thin T_{NS} raises subband energy (Eq. (9)); roughness scattering	Thickness and gate-stack co-optimization (a research need; see Section 10)	V_T shift; mobility

The mitigations are partial Several of the single-module demonstrations in Table IV are not complete fixes, and yield and process-window limits are rarely documented by manufacturers beyond a high level. The best public starting points are the process review and the reliability review [14],[8].

9. NEXT-GENERATION TRANSISTORS AND EMERGING APPLICATIONS

Statements about technology readiness require explicit categories. Commercially used (reported by the companies): nanosheet processes from Samsung [5], TSMC [6] and Intel [7]. Published platform papers include TSMC's 2 nm platform [19] and Intel's 18A platform [20]. Demonstrated research prototypes: stacked NMOS-on-PMOS nanoribbons [13], backside power delivery on a product-like test chip built in a FinFET process [18]. Simulation predictions Forksheet advantages TCAD predictions [11]. The sources cited do not give a schedule for introduction of CFET.

AI and HPC. Higher drive current per footprint and continuous width tuning are relevant to accelerator and server processors, and nanosheet design considerations for HPC appear in [16]. TSMC and Intel frame their 2 nm-class and 18A platforms around AI and HPC use [19], [20].

Mobile and edge. The MBCFET was positioned for low-power and high-performance use with reduced supply voltage as a goal [4].

Mixed-signal. Continuous width selection may ease analog sizing relative to fin quantization [4], but the cited sources report no analog circuit results.

Standard cells and stacking. Simulation projects that the forksheet's tighter n-to-p spacing reduces standard-cell height [11], and CFETs aim to remove the n-to-p spacing limit by stacking [12], [13].

Backside power. Moving power wiring to the wafer backside freed front-side routing resources and gave a voltage-droop improvement above 30% and a 6% frequency benefit on an Intel 4 FinFET test chip [18]. Because the benefit was shown with FinFETs, it is a power-delivery effect and not a nanosheet effect, which is why a product's gain should not be credited to transistor architecture alone. Node-level claims call for the same caution [5], [7].

10. RESEARCH GAPS AND FUTURE DIRECTIONS

The gaps below follow from sections 3-9. Each of them links a challenge to a method and a measurable goal. Objectives are expressed relative to a baseline measured in the same flow, since the sources quoted do not give comparable absolute targets. None of them assumes that a new architecture is better and all of them require comparative evidence.

R1. **Nanosheet geometry and stacking arrangement**. Method: TCAD sweeps of N_{sheet}, W_{NS}, T_{NS}, and T_{sp} calibrated to measured devices. Objective: maximize I_{on}/footprint at fixed I_{off} and bounded capacitance vs baseline stack.

R2. **Electrostatics at aggressive scales** Method: combine models of the type of Eq. (4) with three-dimensional simulation including confinement. Objective: keep SS and DIBL within a stated limit at the minimum L g and T_{NS} the process can support.

R3. **Contact and Source/Drain Engineering**. Method: Contact resistivity and wrap-around contacts test structures [3] Objective: To reduce extrinsic resistance for the same parasitic capacitance.

R4. **Capacitive parasitics and self-heating**. Method: electrothermal simulation and thermometry on test structures [9], [23]. Objective: to reduce the temperature rise per unit power in relation to baseline layout.

R5. **Design with variability awareness**. Method: statistical TCAD and compact models from nanowire studies [2] to stacked sheets. Objective: quantify and then minimize the $\sigma(V_T)$ and $\sigma(I_{on})$ across sheets.

R6. **High activity and temperature stability.** Method: combined BTI, HCI and self-heating stress under realistic switching [8], [17]. Objective: provide lifetime margin at the maximum operating temperature.

R7. **Co-optimization of device, cell, interconnect and power delivery**. Method: Design-technology co-optimization including backside power [18], [11], [19]. Goal: Achieve better power, performance, and area compared to a nanosheet baseline with matched assumptions.

R8. **Independent benchmarking of HPC** Method: The same HPC block in nanosheet and FinFET is compared under matched design rules, supply, temperature, and workload. Objective: Report energy per operation and sustained frequency with stated uncertainty. This would replace the assessment in Section 3.4 with measured evidence.

R9. **Stacked architectures integration**. Method: process-module development for isolation between stacked devices and for stacked contacts with thermal and yield analysis [13], [12]. OBJECTIVE: Raise top and bottom device yield in CFET test vehicles to the level of nanosheet-only flows.

11. CONCLUSION

GAA-nanosheet transistors extend the gate wrap of the FinFET to all channel faces and enable continuous width tuning and a higher effective width per footprint [3], [4]. The first order analysis rationalizes why: natural length decreases with increasing effective gate count (Fig. 4) and enables shorter channels for the same electrostatic control. Good electrostatics have been demonstrated at short gate length [3] and volume production is reported by manufacturers [5],[6],[7]. Section 3 outlines a timeline for a field that started with concept in 2000 and 2003, evolved to platform modules in 2019, and will expand to HPC-oriented platforms in 2024 and 2025. Remaining difficult issues are sheet release and inner-spacer control, bottom-sheet leakage, parasitic resistance and capacitance, self-heating and reliability [14], [8], [22].

Forksheets and CFETs attempt to extend scaling by reducing n-to-p spacing or stacking complementary devices [11], [12], [13]. The evidence they provide is simulation or early demonstration, so the claims of power-performance-area advantage are still tentative. It has been shown that backside power is independent of the transistor architecture [18]. The record suggests that nanosheets will be the first to mature, with forked or stacked variants appearing once process, thermal and reliability issues are resolved. It does not support fixed schedules or performance rankings. In the absence of an independent HPC benchmark, applicability of nanosheets to HPC is a reasoned assessment, not yet measured.

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